REMARKS

Claims 1-15 are pending. Claims 1 and 2 have been amended. No new matter has been added. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. Allowable Subject Matter

Claims 6-15 have been allowed.

Claims 2-5 were objected to as being dependent upon a rejected base claim. The applicant has amended claim 2 to include all the limitations of claim 1. Claims 3-5 depend from claim 2. The applicant respectfully submits that claims 2-5 are in condition for allowance.

II. The §102 Rejections

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,876,683 (Suzuki).

Claim 1, as amended, recites receiving a combined clock-data stream according to a first clock domain, and dividing the combined clock-data stream into independent clock and data streams. Claim 1 further recites synchronizing the independent data stream to a second clock domain for processing by a framer array, recombining the independent data stream and the independent clock stream to form a recombined clock-data stream, and re-synchronizing the recombined clock-data stream to the first clock domain.

Suzuki discloses a repeater for regenerating a frame-multiplexed signal (see Abstract). Referring to FIG. 1 of Suzuki, while Suzuki may disclose extracting a timing signal (e.g., CLK_i) from a demodulated data signal (e.g., $DATA_i$), Suzuki fails to disclose synchronizing the independent data stream to a second clock domain for processing by a framer array, and then re-synchronizing a recombined clock-data stream to the first clock domain.

As acknowledged by the Examiner, Suzuki discloses a frame generation circuit 15 that regenerates a frame-multiplexed signal using a master clock (CLK_m), which is different from a receiving clock signal (CLK_i), however, Suzuki fails to disclose re-synchronizing the

regenerated frame-multiplexed signal to the first clock domain -- e.g., CLK_i. Instead, Suzuki discloses regenerating the frame-multiplexed signal "having a same frequency as the output of selector switch 13". (Col. 2, ll. 42-44). That is, if the output of the selector switch 13 is the master clock CLK_m, then the frame generation circuit will regenerate the frame-multiplexed signal to have a same frequency as that of the master clock signal CLK_m. Likewise, if the output of the selector switch 13 is the receiving clock CLK_i, then the frame generation circuit will regenerate the frame multiplexed signal to have a same frequency as that of the receiving clock CLK_i. Suzuki, therefore, fails to disclose synchronizing the independent data stream to a second clock domain for processing by a framer array, and then re-synchronizing a recombined clock-data stream to the first clock domain, as required by claim 1. The applicant respectfully submits that claim 1 is, therefore, allowable over Suzuki.

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Respectfully submitted,

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